ABSTRACT OF THE DISCLOSURE

Information of priorities of a plurality of tasks and orders-per-priority has been stored in a matrix circuit (1). A priority encoder (2) extracts a value of the highest priority from the matrix circuit (1). This value is held in a priority register (18). An order-per-priority control circuit (6) sets the value of the highest order among the orders-per-priority into an order register 19 and sets this value so that it is set to the lowest order when it is read out next. A task executing unit (20) reads out an address of the task to be executed next from the priority register (18) and order register (19), executes the task, and after the execution, updates the information in the matrix circuit 1 on the basis of a state of the task. A plurality of tasks can be switched at a high speed.